ABSTRACT:

Reliability and Stress-Related Phenomena – From the PC era to the AI era

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In the PC era, the reliability of back-end-of-line (BEoL) structures - Al-based metallizations and SiO_2 insulating dielectrics - was dominated by electromigration (EM)-induced voiding and hillock formation, with stress-induced voiding (SIV) arising from thermo-mechanical stress built up during BEoL processing as a secondary concern. The shift to Cu dual-damascene interconnects introduced new stress-related failure mechanisms. The integration of low-permittivity (low-k) dielectrics reduced the mechanical robustness of Cu/low-k stacks and increased the risk of time-dependent dielectric breakdown (TDDB). Cu microstructure, Cu/low-k interface, and stress engineering were needed to avoid EM failure and mechanical failure caused by microcracks. Diffusion-barrier and liner integrity became critical for EM and SIV as interconnect dimensions continued to shrink.

The AI era has intensified all these phenomena. Advanced packaging technologies and chiplet architectures, combined with aggressive scaling, push current density, as well as local stress and temperature gradients, to unprecedented levels, accelerating the degradation processes described above. Microcracks caused by thermal-cycling fatigue in solder microbumps and fine-pitch Cu–Cu hybrid bonds are new failure modes.

This talk reviews the physics of degradation and failure, characterization techniques, and modeling and simulation of stress-related phenomena in metal interconnects. Reliability engineering for AI-era interconnect stacks requires coupled multiphysics models and advanced, high-resolution, nondestructive 3D imaging to study the kinetics of reliability-limiting processes in integrated circuits. Emerging approaches will include more robust low-k dielectrics, barrier/liner redesign, Ru-based subtractive interconnects, and air-gap architectures. A future challenge will be predictive reliability assessment in next-generation 3D-integrated and chiplet architectures.